

ABSTRACT

The invention describes a structure and a process for providing ESD semiconductor protection with reduced input capacitance. The structure consists of a heavily doped P+ contact area residing in an N well region on a P substrate and electrically connected to the input pad of active integrated field effect transistor devices. NFET devices with floating gates and drains to reduce capacitance are located in the substrate near the N-well. The NFET source elements as well as the substrate are connected to ground. The NFETs are isolated from the N-well and associate P+ contact area by shallow trench isolation (STI) structures that reduce the NFET drain to substrate and N-well to substrate junction boundary area with a subsequent reduction in the junction capacitance. A voltage pulse from an ESD event will cause the SCR structure and associated parasitic bipolar transistors to trigger providing a path to ground for the ESD current, thereby protecting the internal circuits from damage.